



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,627	12/19/2005	Andrei Terechko	NL02 1504 US	8431
65913	7550	09/05/2008	EXAMINER	
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			BAE, JI H	
			ART UNIT	PAPER NUMBER
			2115	
			NOTIFICATION DATE	DELIVERY MODE
			09/05/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary**Application No.**

10/561,627

Applicant(s)

TERECHKO ET AL.

Examiner

JI H. BAE

Art Unit

2115

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 June 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 12-21 is/are rejected.
- 7) ☒ Claim(s) 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/CDC)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____
- Paper No(s)/Mail Date _____

DETAILED ACTION

Response to Arguments

Applicant's arguments, see applicant's appeal brief, filed on 23 June 2008, with respect to the rejection(s) of claim(s) 1-21 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 14 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 14 recites program product comprised of a hardware definition program and a signal bearing medium that bears the hardware definition program, wherein the signal bearing medium comprises a transmission medium. Transmission media include digital and analog communication links as described by the applicant [specification pp. 10, lines 10-14], and as such are understood to include propagated signals. Propagated signals do not fall within any of the statutory categories for invention, nor do they represent a judicial exception with either a physical transformation or a useful, concrete, and tangible result. Therefore, the claimed subject matter is deemed to be non-statutory.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2115

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka, U.S. Patent No. 4,733,346, in view of Gupta, U.S. Patent No. 5,996,083.

Regarding claim 1, Tanaka teaches a circuit arrangement comprising:

a register file partitioned into a plurality of banks **[Fig. 1, register blocks 12a, 12b, and 12c]**, each bank including at least one register and at least one address input and data input **[Fig. 5 and 6, CPU interfaces with register block via data bus 22D and address bus 22A, col. 6, line 58 to col. 7, line 25]**; and

enable logic coupled to the register file and configured to selectively disable at least one unused bank from the plurality of banks by gating off the address and data inputs thereof **[Fig. 5 and 6, transistors 92 and 98, controlled by control line 26A; col. 8, lines 66-67, register block set to state C cannot be accessed by CPU; col. 10, lines 4-26, control signal 26A enables CPU access to register]**.

Tanaka does not teach gating clock inputs to the register banks.

Gupta teaches a system wherein a power control register is set based on examining an instruction stream, and determining when a functional unit will be unused **[col. 3, lines 40-63]**. The power control register settings can be used to gate a clock signal from an unused functional block **[Fig. 4, col. 7, lines 1-20]**.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Tanaka and Gupta by implementing the clock gating logic of Gupta in the system of Tanaka. Tanaka teaches a system wherein a register block may be placed in a state where it cannot be accessed by the CPU **[state "C"]**, and further teaches that the address and data bus are connected to the register block by transistors that are controlled based on the state. In Fig. 9 of

Tanaka, it is observed that register block 12B is placed in state C after being in state E but before state D. In state D, a value is written to the register by the CPU for storage into memory, while in state E another value is written to the register by the memory for reading by the CPU [col. 8, line 66 to col. 9, line 2]. Therefore, when register block 12B is in state C, it is unused because 1) it is not accessible to the CPU, and 2) the current value held in the register is about to be overwritten based on the change in state.

Gupta teaches a system for saving power when a functional block of system is unused by gating off the clock inputs based on an examination of the instruction stream. Although Tanaka does not explicitly disclose clock inputs to the register block, the examiner submits that registers require a clock signal, and therefore must be present although not explicitly disclosed. Given this, it would have been obvious to combine the teachings of Gupta with the system of Tanaka. The motivation to combine would have come from Tanaka's teaching that the register block is unused during the state "C", and Gupta's disclosure that it would be desirable to gate clock inputs to unused functional blocks in order save power.

Regarding claim 2, Tanaka teaches that the register blocks are comprised of a CMOS flip-flop or latch [col. 6, lines 62-64, one-bit registers].

Regarding claim 3, Tanaka teaches a plurality of enable circuits coupled to the register bank, each enable circuit configured to gate off address and data signals [Fig. 5 and 6, transistors 92 and 98]. Gupta teaches an enable circuit for gating the clock signals [Fig. 4].

Regarding claim 4, Tanaka teaches that the enable circuits are transistors, each transistor controlled by an enable signal [Fig. 5 and 6, control signal 26].

Regarding claim 5, Tanaka teaches output select logic for the plurality of register banks [Fig. 5 and 6, transistors 94 and 98 and control signal 28].

Regarding claim 6, Tanaka teaches that the enable logic dynamically determines which register banks are unused and generates an enable signal based on the determination **[Fig. 3, logic generates control signal 26A]**.

Regarding claim 7, Tanaka teaches an address decoder for generating enable signals responsive to an address specified by address inputs **[Fig. 6, binary decoder 95, address bus inputs 22A]**.

Regarding claims 8-10, Gupta teaches a support register for storing power modes state information, wherein the support register is updated responsive to a power control instruction resident in program code **[Fig. 4, power control register 106, col. 5, lines 60-65, power control register set by software]**.

Regarding claims 12 and 13, Tanaka teaches a processor system disposed on an IC **[Fig. 1, processor 1]**.

Regarding claims 15-21, Tanaka/Gupta teaches the circuit arrangement of claim 1-10 and 12-13. Tanaka/Gupta also teaches the method that is carried out by the claimed circuit arrangement.

Allowable Subject Matter

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JI H. BAE whose telephone number is (571)272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JI H. BAE/
Examiner, Art Unit 2115
U.S. Patent and Trademark Office
571-272-7181
ji.bae@uspto.gov